Description

CM1602A is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

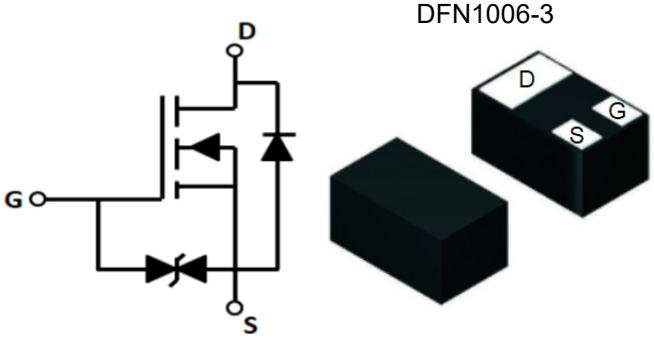
- VDS: 20V
- ID: 0.9A
- RDSON(@VGS=4.5V) : < 250mΩ
- RDSON(@VGS=2.5V) : < 350mΩ
- High density cell design for extremely low RDSON
- Excellent on-resistance and DC current capability

Applications

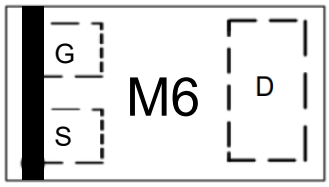
- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Dimensions and Pin Configuration

DFN1006-3



Marking Information



M6 = Device Marking Code

Ordering Information

Part Number	Marking	Packaging	Reel Size
CM1602A	M6	10000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	±10	V
Continuous Drain Current	T_A=25°C , t≤5s	I_D	1	A
	T_A=25°C , Steady State		0. 9	A
	T_A=75°C ,Steady State		0.69	A
Pulsed Drain Current[1]		I_{DM}	4.0	A
Total Power Dissipation @ T_A=25°C [2]	t≤5s	P_D	430	mW
	Steady State		340	
Thermal Resistance Junction-to-Ambient [2]	@t≤5s	$R_{\theta JA}$	294	°C/W
Thermal Resistance Junction-to-Ambient [2]	@Steady State		366	
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V			±10	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.35	0.75	1.1	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=0.5A		190	250	mΩ
		V_{GS}=2.5V,I_D=0.45A		270	350	
Diode Forward Voltage	V_{SD}	I_S=0.6A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				0.9	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=16V,V_{GS}=0V,f=1MHz		26		pF
Output Capacitance	C_{oss}			9		
Reverse Transfer Capacitance	C_{rss}			5		
Switching Parameters						
Total Gate Charge	Qg	V_{GS}=4.5V,V_{DS}=10V, I_D=0.5A		0.84		nC
Gate Source Charge	Qgs			0.25		
Gate Drain Charge	Qgd			0.10		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V, I_D=0.5A,R_{GEN}=10Ω		2		ns
Turn-on Rise Time	t_r			18.8		
Turn-off Delay Time	$t_{D(off)}$			10		
Turn-off Fall Time	t_f			23		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6cm^2.

Typical Performance Characteristics (T_A=25℃ unless otherwise Specified)

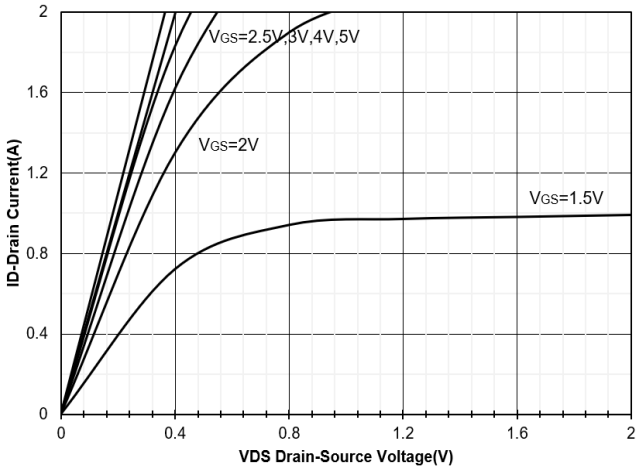


Figure 1. Output Characteristics

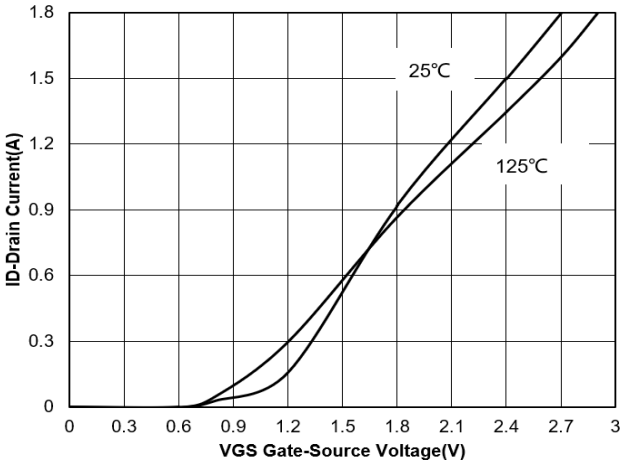


Figure 2. Transfer Characteristics

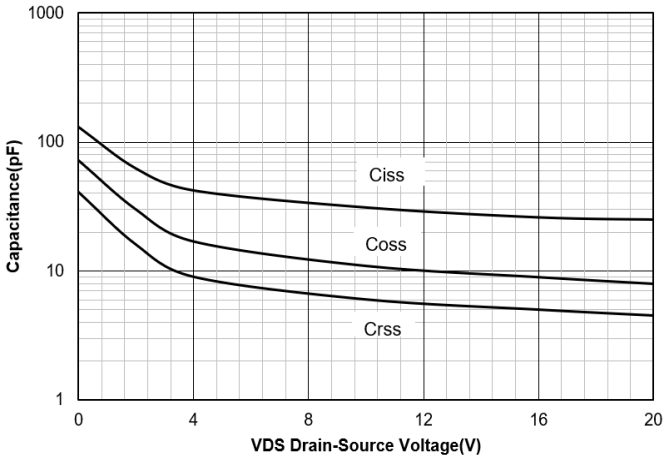


Figure 3. Capacitance Characteristics

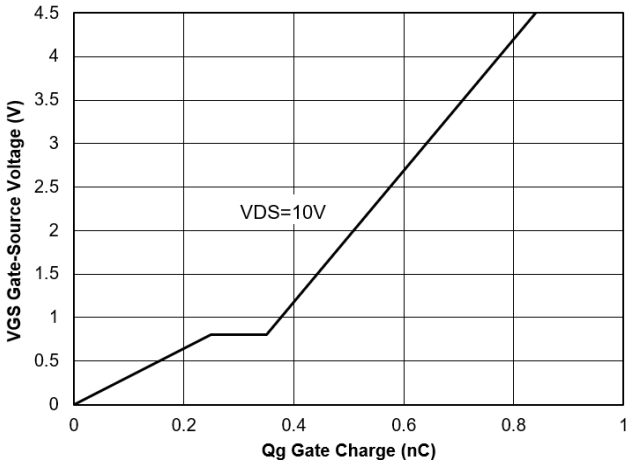


Figure 4. Gate Charge

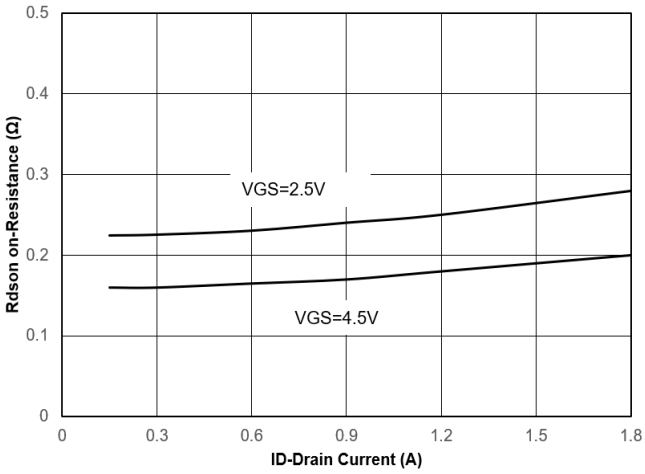


Figure 5. Drain-Source on Resistance

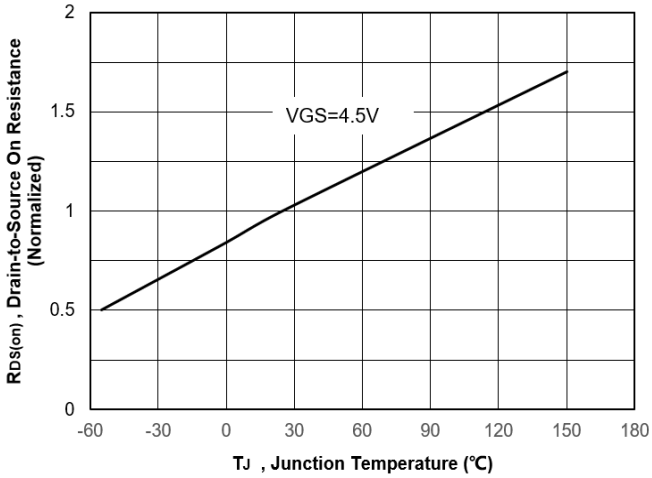


Figure 6. Normalized On-Resistance Vs. Temperature

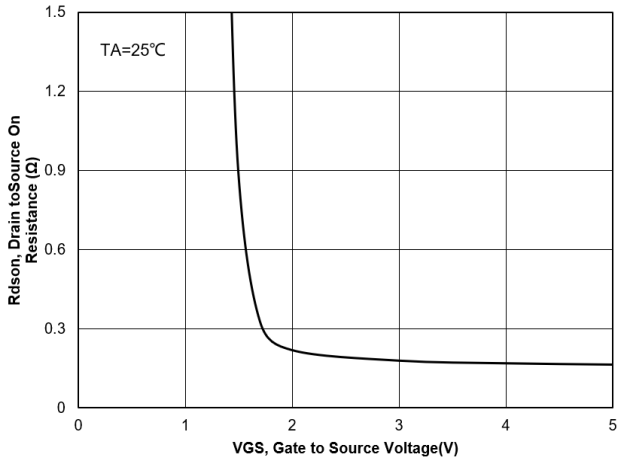


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

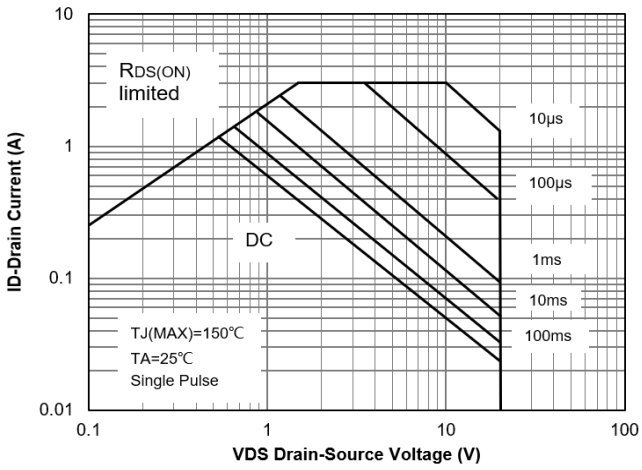


Figure 8. Safe Operation Area

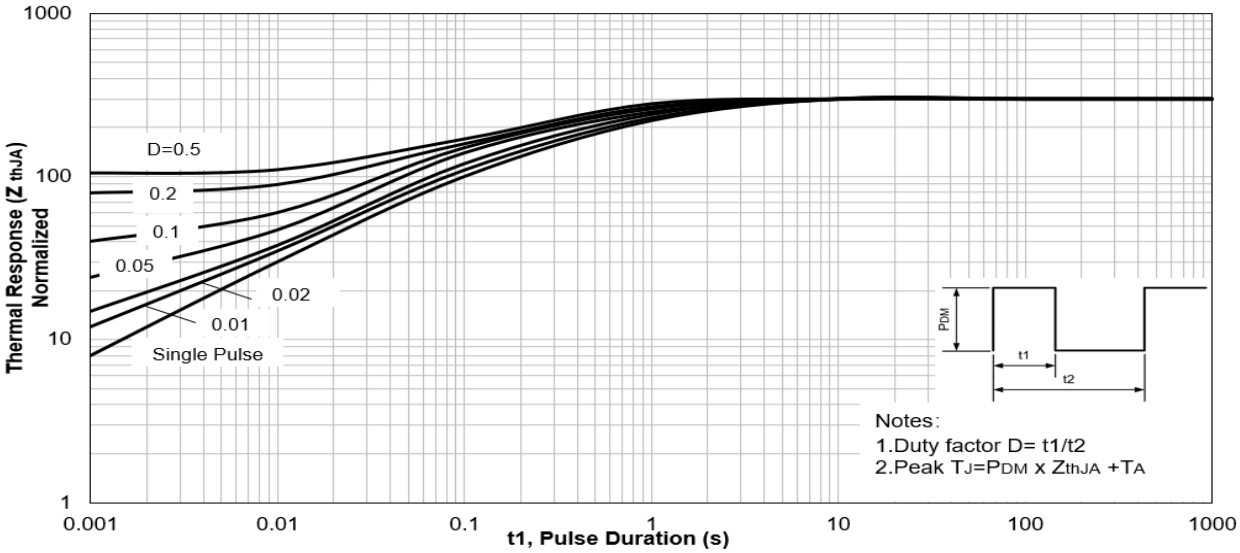


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

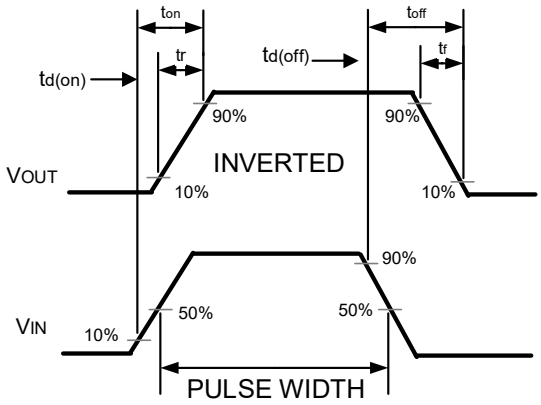
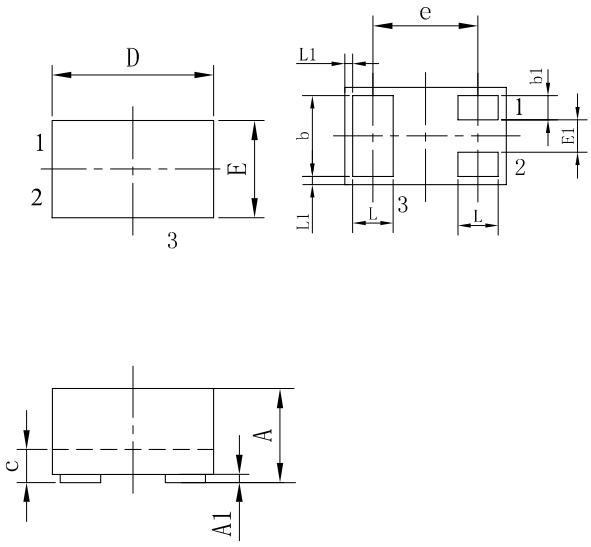


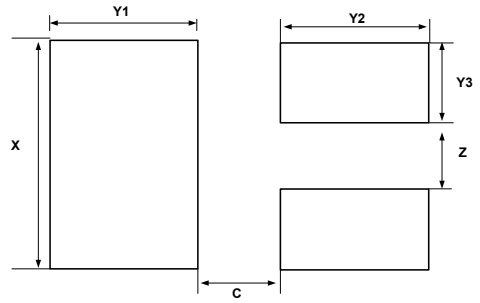
Figure 10. Switching wave

DFN1006-3 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	0.10	0.15	0.20	0.004	0.006	0.008
c	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
E1	0.15	0.20	0.25	0.006	0.008	0.010
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05 REF			0.0002 REF		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	0.25	0.010
X	0.65	0.024
Y1	0.50	0.020
Y2	0.50	0.020
Y3	0.25	0.010
Z	0.20	0.008

Contact Information

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